ADQ3-FWATD Datasheet

The ADQ3-FWATD is an averaging firmware of the high-end ADQ3 series of digitizers. The FWATD is designed to maximize the signal to noise ratio in pulse data systems.

Ordering information

- ADQ3 digitizer including firmware FWATD, order code **ADQ3-FWATD**.

Compatible hardware models

- ADQ30 single-channel mode
- ADQ32 single- and dual-channel modes
- ADQ32-PDRX combined channels and dual-channel mode (not combined)
- ADQ33 dual-channel mode
- ADQ33-PDRX combined channels and dual-channel mode (not combined)
- ADQ35 single- and dual-channel mode

1 ADQ3-FWATD INTRODUCTION

1.1 Features

- Accumulation of waveforms at high duty cycle
- Background streaming of data, no dead-time between accumulation
- DBS – digital baseline stabilizer to reduce pattern noise
- Digital FIR filter for bandwidth limitation
- Sample skip support to increase measurement length
- Threshold function for suppressing noise
- FIR filter for threshold control enables pulse shape selection
- Dual gain PDRX firmware in combination with averaging (separate license may apply)

1.2 Applications

- Time-of-flight Mass Spectrometry
- Distributed Optical Fiber Sensing
- Noise reduction of repetitive measurements
- Pulse data applications

1.3 Advantages

- Efficient implementation of averaging in the FPGA off-loading the PC
- Four noise reduction methods
    - Digital Baseline Stabilizer (DBS)
    - FIR filter for noise filtering
    - Threshold for noise cancellation
    - Averaging for noise reduction
- Optimized for real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2 FOUR NOISE SUPPRESSION METHODS – PRINCIPLE OF OPERATION

2.1 DBS – Digital Baseline Stabilizer

The DBS analyses the signal and subtracts DC offset. This creates a solid reference point for computing pulse-related parameters. The DBS actively compensates for slow baseline shifts as temperature variations, supply voltage drift and aging and stabilizes the baseline to a level corresponding to 22 bits precision.

The DBS also compensates for pattern noise in interleaved ADCs. This is important when averaging very long sequences since the pattern noise may drown weak signals.

2.2 General purpose FIR filter

The general-purpose FIR filter enables the suppression of noise in a certain frequency band. The FIR filter is user-controlled so that it can be optimized for the specific application/system.

2.3 Threshold with FIR filter

Threshold operation sets samples below a user-defined level, *t*, to a user-controlled register value, *z*, (often 0). The threshold function can be tuned with a filter to emphasize certain pulse shapes by the threshold filter function. The operation is like follows:

1. The sequence of samples is [$x_0\ x_1\ x_2 \ldots x_n$].
2. Apply the threshold filter on the sequence of sample to get [$f_0\ f_1\ f_2 \ldots f_n$].
3. The conditions are then:

a. for each sample *f* which is below the threshold *t*, set register value *z*.
b. for each sample *f* which is above the threshold *t*, maintain the value of *x*.

This example is for positive signals. The threshold operation works for both negative and positive signals.

2.4 Accumulator

The accumulator adds records (waveforms) to each other. The noise is assumed to be uncorrelated and the signal is assumed to be correlated. The accumulation then enhances the signal to noise ratio. An example of operation is:

The first record, r_0, contains the series of samples [$x_{00}\ x_{01}\ x_{02} \ldots x_{0n}$], where x_{00} is the first sample. Following records are r_1 = [$x_{10}\ x_{11}\ x_{12} \ldots x_{1n}$] and r_2 = [$x_{20}\ x_{21}\ x_{22} \ldots x_{2n}$]. The accumulator result for adding these records is then the series [$(x_{00}+x_{10}+x_{20})\ (x_{01}+x_{11}+x_{21})\ (x_{02}+x_{12}+x_{22}) \ldots (x_{0n}+x_{1n}+x_{2n})$].

If the division part of the averaging function is required, it must be implemented in the user's application software.

3 SYSTEM DESIGN USING FWATD

3.1 Fundamental observations

The environment where FWATD is used is a real-time operating measurement system. The signals detector and the digitizer operate in a real-time domain. The data is analyzed in a PC, which is not real-time controlled. Certain design steps have been taken in the FWATD to handle the transition for the real-time domain into the PC in a safe way.

3.2 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ3-series offers a variety of options for efficient system design:

The FWATD firmware implements the most demanding core of the processing in the FPGA. Data from the processing is streamed to a PC using the high-speed streaming interface.

The streaming of data proceeds in parallel with the recording. There is thus no dead-time introduced by data transfer.

There are many parameters to tune for optimal performance. See the ADQ3 series user guide for instructions.

3.3 Scheduling for high performance and data safety

The FWATD is suitable for a system with a strict scheduled operation. The dataflow is driven by the trigger, internal from the digitizer or external from the signal source. The user must make sure that all data transport and processing is fast enough to handle the data rate.

The FWATD firmware is designed to operate constantly over long time in a system which maximizes the performance. The FWATD firmware contains multiple features to support the data transport and processing.

1. There is a FIFO on the digitizer to manage unexpected interrupts in the PCIe data transport.
2. There is a controlled data discard in case of an overflow due to interrupts anywhere in the processing chain.
3. There is an auto-recover and re-synchronize feature in case of lost data. This is useful for very long measurement operations. In case of an unexpected interrupt in the data transport which cannot be handled by the FIFO, the FWATD firmware maintains the grid established by the trigger source and the accumulation factor and ensures that the following accumulations are not affected. It is not necessary to restart the system to continue the measurement.
4. The data read-out is thread safe and multiple threads can operate on the data. This increases the processing capacity of the system.

4 TECHNICAL DATA

Table 1 Software support

Parameter	Value
Operating system[1]	Windows 10 / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

Table 2 Hardware models

Digitizer model	Sampling rate per channel	Channels	Max Record length[2]	Max data transfer rate[3] [4]
ADQ33	1 GSPS	2	500 ms	7 GBPS
ADQ33-PDRX	1 GSPS	1	500 ms	7 GBPS
ADQ33-PDRX	1 GSPS	2	500 ms	7 GBPS
ADQ32	2.5 GSPS	2	200 ms	7 GBPS
ADQ32	5 GSPS	1	200 ms	7 GBPS
ADQ32-PDRX	2.5 GSPS	1	200 ms	7 GBPS
ADQ32-PDRX	2.5 GSPS	2	200 ms	7 GBPS
ADQ30	1 GSPS	1	500 ms	7 GBPS
ADQ35	5 GSPS	2	200 us	14 GBPS
ADQ35	10 GSPS	1	200 us	14 GBPS

[1] See 15-1494 Operating system support for a detailed listing of supported distributions.
[2] If sample skip is used the record length is increased in the same degree as samples are skipped.
[3] This is the rate supported by the digitizer hardware. The effective data rate may be limited by components in the system.
[4] Using averaging reduces the actual data rate. The data rate can be approximated as *trigger_rate [Hz] * record_length [samples] * 4 [bytes/sample] / number of accumulations*.

Table 3 General parameters

Parameter	Min	Max	Unit
FIR filter general purposes [5]	1	17	taps
FIR filter for threshold operation [5]	1	17	taps
Number of accumulations [6]	1	262 144	
Re-arm time between records [7]	20		ns
Dead time between accumulations [7]	20		ns
Data format	8 / 16 / 32		bits

5 CHANGING NUMBER OF CHANNELS

Some hardware models support both one and 2 channels operation. Changing from 2 channels to 1 channel is done by changing firmware image in the FPGA. Both firmware images are stored in the non-volatile memory of the digitizer. Use the software tool ADQAssist to change boot image. Changing firmware requires power cycling of the PC for the PCIe bus to enumerate.

[5] The filter is symmetrical so there are 9 unique coefficients.
[6] This is limited by the 32-bit data format from the digitizer. Since the accumulations are seamless, the user can convert data to 64-bit format and continue the accumulation to almost any number of records.
[7] Re-arm time between records are well as dead-time between accumulations is 20ns. This means that a new accumulation can be started seamlessly without any loss of data. If the number of accumulations is small, an increased dead-time may be necessary to meet the data transfer requirements.

6 BLOCK DIAGRAM

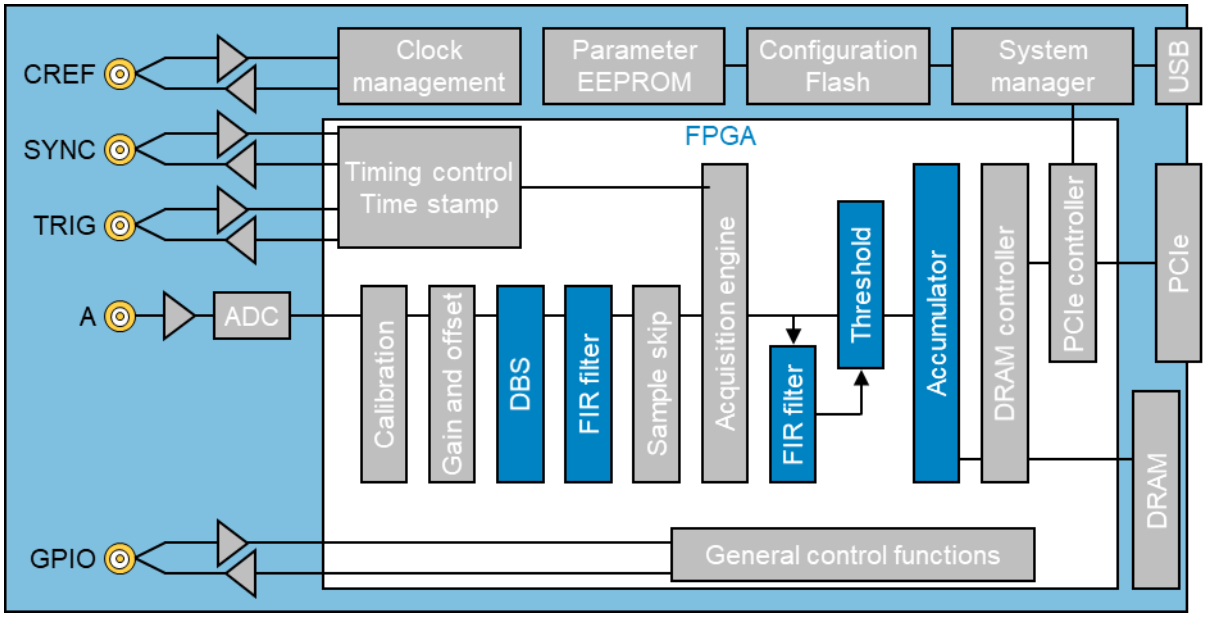

Figure 1 Block diagram for a single channel digitizer.

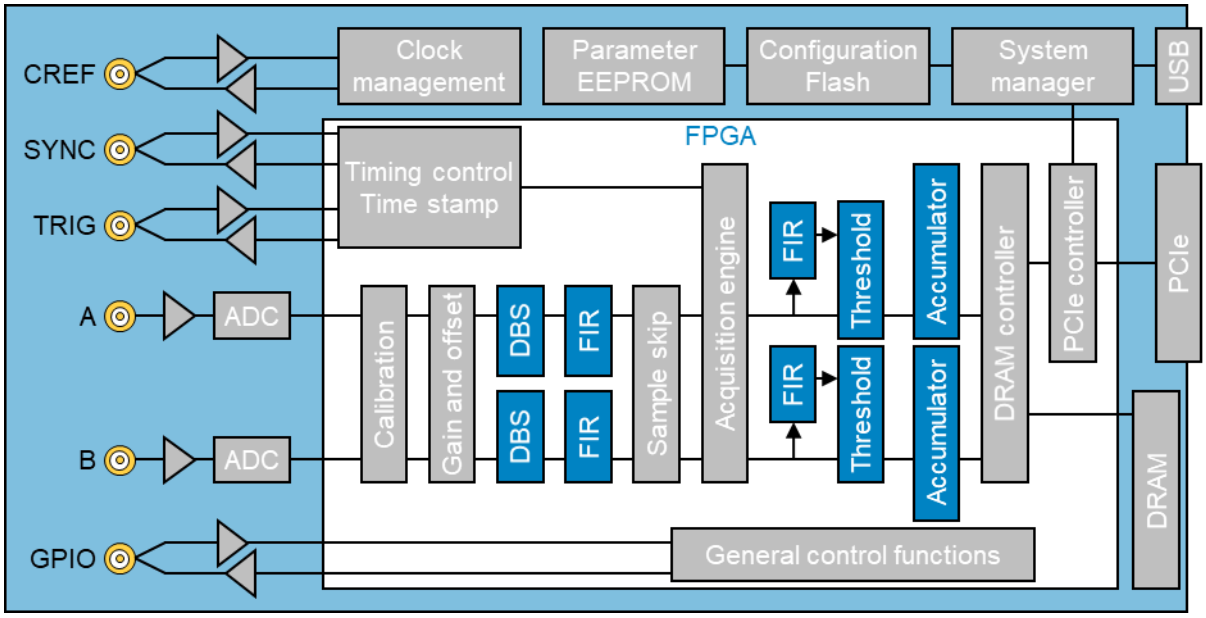

Figure 2 Block diagram for a dual channel digitizer

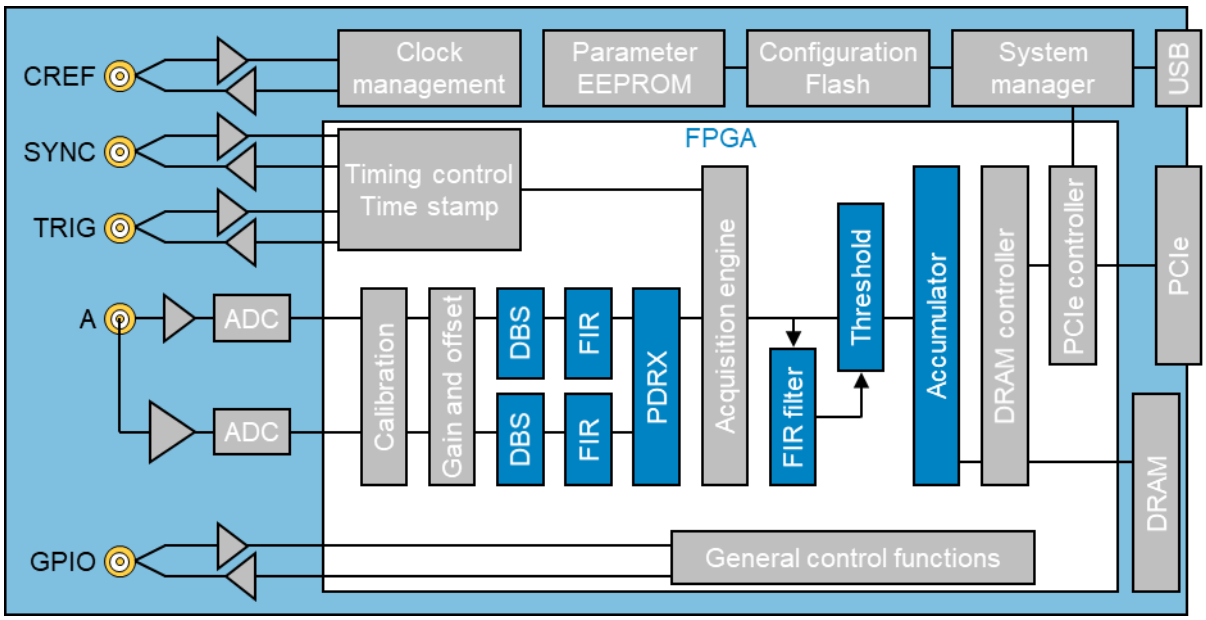

Figure 3 Combined with PDRX (requires PDRX license)

Figure 4 Typical digitizer in the ADQ3 family

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www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 8
SE-583 30 Linköping
Sweden
Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com